APPARATUS AND METHOD OF DRIVING HIGH-EFFICIENCY PLASMA DISPLAY PANEL

BACKGROUND OF THE INVENTION

[01] This application claims priority from Korean Patent Application No. 2002-69256, filed on November 8, 2002, in the Korean Intellectual Property Office, the disclosure of which is incorporated herein in its entirety by reference.

1. Field of the Invention

[02] The present invention relates to an apparatus and a method of driving a plasma display panel (PDP), and more particularly, to an apparatus and a method of driving a high-efficiency PDP for quickly eliminating a free-wheeling current, which is generated due to the parasitic effect in an energy recovery circuit, and improving the energy recovery efficiency.

2. Description of the Related Art

[03] In general, a plasma display panel (PDP) is a flat display for displaying characters or images using plasma generated by gas discharge. Pixels ranging from several hundreds of thousands to more than millions, according to the size of the PDP, are arranged in the form of a matrix.

[04] FIG. 1 shows a conventional alternating current (AC) – PDP sustain-discharge driver suggested by L.F. Weber, which includes an energy recovery unit with a clamping diode for suppressing the surge voltages of switches S_r, S_s, S_f, and S_d. The panel is assumed to have capacitor C_p as a load to analyze PDP driving circuit. FIG. 2 shows graphs of an output panel voltage V_p and a current I_L flowing through an inductor L, according to a switching sequence. The AC - PDP sustain-discharge driver operates in the following four modes, according to the switching sequence.

1) Mode 1

[05] A both-end panel voltage V_p is sustained at 0V when a switch S_{x2} (not shown; a metal-oxide-semiconductor field effect transistor (MOSFET) corresponding to the switch S_d of a side 2 sustain-discharge driver) is turned on just before the switch S_r functioning as the MOSFET is turned on. Once the switch S_r is turned on, the AC – PDP sustain-discharge driver begins to operate in mode 1. In mode 1, an LC resonance circuit is formed through a path of the energy recovery capacitor C_c, the switch S_r, the diode D_r, the inductor L, and the capacitor C_p, as shown in FIG. 3A. Therefore, the current I_L flows through the inductor L and the output voltage V_p of the panel increases. As a result, the current I_L flowing through the inductor L becomes 0A, and the output voltage V_p of the panel becomes voltage $+V_{pk}$.

2) Mode 2

[06] In mode 2, the switch S_r is turned off, and the switch S_s is turned on. The both-end voltage at switch S_s is changed from the voltage $+V_{pk}$ to the voltage $+V_s$, which causes switching voltage loss. The voltage difference between the voltage $+V_{pk}$ and the voltage $+V_s$ is due to the parasitic components of the driver, such as parasitic capacitors or parasitic resistances. As shown in FIG. 3B, this voltage difference between the voltage $+V_{pk}$ and the voltage $+V_s$ causes a free-wheeling current that flows through a path of the switch S_s, the inductor L, and the diode D_1. As shown in FIG. 2, the free-wheeling current decreases slowly because the both-end voltage at inductor L becomes about 2V, i.e., the voltage drop level of the diode D_1 and the switch S_s. In mode 2, the output voltage V_p of the panel is sustained at the voltage + V_s, and the discharge of the panel is sustained.

3) Mode 3

[07] In mode 3, the switch S_f is turned on and the switch S_s is turned off. The LC resonance circuit is formed through a path of the capacitor C_p, the inductor L, the diode D_f, the switch S_f, and the energy recovery capacitor C_c. Therefore, the current I_L flows through the inductor L, and the output voltage V_p of the panel decreases. As a result, the current I_L flowing through the inductor L becomes 0A and the output voltage V_p of the panel becomes equal to the voltage difference between the voltage $+V_{pk}$ and the voltage $+V_s$.

4) Mode 4

[08] In mode 4, the switch S_d is turned on and the switch S_f is turned off. The both-end voltage at switch S_d is changed from the voltage V_s - V_{pk} into 0V rapidly, which causes switching loss. The voltage difference between the voltage $+V_{pk}$ and the voltage $+V_s$ is due to the parasitic components of the driver, such as parasitic capacitors or parasitic resistances. As shown in FIG. 3D, this voltage difference between the voltage $+V_{pk}$ and the voltage $+V_s$ causes the free-wheeling current which flows through a path of the diode D_2, the inductor L, and the switch S_d. As shown in FIG. 2, the free-wheeling current decreases slowly because both-end voltage at the inductor L becomes about 2V, i.e., the voltage drop level of the diode D_2 and the switch S_d.

[09] Thereafter, the switch S_{x2} is turned off, and a switch S_{x1} (not shown; a MOSFET corresponding to the switch S_r of a side 2 sustain-discharge driver) is turned on. Then, the process returns to the operation of mode 1, and the operations of mode 1 through 4 are repeated.

[10] However, the free-wheeling current generated in the AC-PDP sustain-discharge driver causes the following problems.

[11] First, since the free-wheeling current is very strong, i.e., about 30A, it increases the stress which is applied to components through which the free-wheeling current flows, such as the switch S_s, the switch S_d, the inductor L, the diode D_1, and the diode D_2. As a result, high-current standard components

must be used in the driver, which increases the size and production cost of the driver.

[12] Second, the free-wheeling current increases the power consumption of the AC-PDP sustain-discharge driver.

[13] Third, the free-wheeling current makes it difficult to control the timing sequence on the rising and falling edges of the output voltage V_p of the panel. In other words, the free-wheeling current hinders the timing sequence control of a gate signal.

SUMMARY OF THE INVENTION

[14] The present invention provides an apparatus and a method of driving a high-efficiency plasma display panel (PDP) for quickly eliminating a free-wheeling current which is generated due to the parasitic effect in the switching sequence of an energy recovery unit.

[15] According to an aspect of the present invention, there is provided a sustain-discharge driving device of a high-efficiency plasma display panel (PDP). The sustain-discharge driving device comprises a sustain-discharge switching unit that connects charging and discharging paths of an energy recovery unit to the PDP, according to a sustain-discharge sequence. The energy recovery unit, according to an energy recovery sequence, discharges energy of the PDP to an energy accumulation device through a resonance path while in discharging mode, charges the PDP with the energy accumulated in

the energy accumulation device through a resonance path while in charging mode, and forms a closed circuit in which a voltage difference between both ends of an inductor is greater than a predetermined value, so as to eliminate a free-wheeling current, which is generated in the inductor of the resonance path due to a parasitic effect, during mode transition.

[16] According to another aspect of the present invention, there is provided a plasma display panel (PDP) driving system which repeats reset, address, and sustain-discharge periods according to a switching sequence. The PDP driving system comprises a Y electrode sustain-discharge driving circuit, a separation and reset circuit, a scan pulse generating circuit, and an X electrode sustain-discharge driving circuit. The Y electrode sustain-discharge driving circuit applies a high frequency voltage of rectangular waveform to a Y electrode of the PDP, by dividing a charging mode into a first charging mode and a second charging mode, and a first discharging mode and a second discharging mode, directs the Y electrode of the PDP to be charged and/or discharged through a resonance path caused by difference inductors in the first and second charging modes, and in the first and second discharging modes, and includes a closed circuit in which a voltage difference between both ends of an inductor is greater than a predetermined value so as to eliminate a free-wheeling current, which is generated in the inductor of the resonance path due to a parasitic effect, during mode transition. The separation and reset circuit separates circuit operations, during the sustain period, from circuit operations,

during other periods such as the address period and the reset period, and applies a ramp-type high voltage to the PDP during the reset period. The scan pulse generating circuit applies a horizontal synchronization signal during the address period, which is shortened during the other periods. The X electrode sustain-discharge driving circuit applies a high frequency voltage of rectangular waveform to an X electrode of the PDP, by dividing a charging mode into a first charging mode and a second charging mode and dividing a discharging mode into a first discharging mode and a second discharging mode, directs the first and second charging modes, and in the first and second discharging modes to charge and/or discharge the Y electrode of the PDP through a resonance path including difference inductors, and includes a closed circuit in which a voltage difference between both ends of the inductor is greater than a predetermined value, so as to eliminate a free-wheeling current, which is generated in the inductor of the resonance path due to a parasitic effect, during mode transition.

BRIEF DESCRIPTION OF THE DRAWINGS

[17] The above and other features and advantages of the present invention will become more apparent by describing in detail exemplary embodiments thereof with reference to the attached drawings in which:

[18] FIG. 1 shows a conventional plasma display panel (PDP) sustain-discharge driver;

[19] FIG. 2 shows graphs of an output voltage V_p of the PDP and a current I_L flowing through an inductor L, according to the switching sequence of an energy recovery unit, in each mode of the conventional PDP sustain-discharge driver of FIG. 1;

[20] FIGS. 3A through 3D show paths through which current flows according to the switching sequence of the energy recovery unit, in each mode of the conventional PDP sustain-discharge driver of FIG. 1;

[21] FIG. 4 shows a sustain-discharge driving device of a high-efficiency PDP according to the present invention;

[22] FIG. 5 shows graphs of switching control signals, a voltage, and a current used in the sustain-discharge driving device of FIG. 4;

[23] FIGS. 6A through 6H show paths through which current flows according to the switching sequence, in each mode of the sustain-discharge driving device of FIG. 4; and

[24] FIG. 7 shows a PDP driving system according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[25] The present invention will now be described more fully with reference to the accompanying drawings, in which preferred embodiments of the invention are shown.

[26] As shown in FIG. 4, a sustain-discharge driving device of a high-efficiency plasma display panel (PDP) according to the present invention includes a sustain-discharge switching unit, an energy recovery unit, and a plasma display panel (PDP).

[27] The sustain-discharge switching unit includes four switches S_{d1}, S_{d2}, S_{u2}, and S_{u1} that are connected in series. One end of the switch S_{d1} is connected to a ground line. One end of the switch S_{u1} is connected to a supply voltage $+V_s$. A contact point of the switches S_{d2} and S_{u2} is connected to a PDP (C_p). A contact point of the switch S_{d1} and the switch S_{d2}, and a contact point of the switch S_{u2} and the switch S_{u1} are each connected to the energy recovery unit.

[28] The energy recovery unit includes an energy accumulation block, a path switching block, a plurality of inductors, and a plurality of diodes.

[29] More specifically, the energy accumulation block includes four capacitors C_{d1}, C_{d2}, C_{u2}, and C_{u1} connected in series. One end of the switch C_{d1} is connected to the ground line. One end of the switch C_{u1} is connected to the supply voltage $+V_s$.

[30] The path switching block includes a plurality of diodes D_{r1}, D_{r2}, D_{f1}, D_{f2}, D_u, and D_d, a plurality of switches S_{r1}, S_{f1}, S_{r2}, and S_{f2} that are connected in parallel to the capacitors C_{d1}, C_{d2}, C_{u2}, and C_{u1}, respectively. The path switching block switches a current path and forms a resonance path through which current flows via different inductors in the first and second charging

modes and the first and second discharging modes, according to an energy recovery sequence.

[31] A plurality of inductors L_{r1}, L_{f1}, L_{r2} and L_{f2} is connected to a plurality of switches S_{r1}, S_{f1}, S_{r2}, and S_{f2} and forms an LC resonance circuit for energy recovery in the first and second charging modes and the first and second discharging modes.

[32] A plurality of diodes D_{u1}, D_{u2}, D_{u3}, D_{u4}, D_{d1}, D_{d2}, D_{d3}, and D_{d4}, while connected to both ends of a plurality of inductors L_{r1}, L_{r2}, L_{f1}, and L_{f2}, clamps the voltages of switches and forms a path for eliminating a free-wheeling current. In other words, a free-wheeling current is generated in the inductor of the resonance path, due to the parasitic effect during mode transitions. When this occurs, a plurality of diodes D_{u1}, D_{u2}, D_{u3}, D_{u4}, D_{d1}, D_{d2}, D_{d3}, and D_{d4} is configured to form a path for discharging the free-wheeling current.

[33] In FIG. 4, the sustain-discharge driving device is represented by only a side 1 electrode of the PDP for the sake of convenience. A side 2 electrode of the PDP is configured in the same manner as the side 1 electrode of the PDP.

[34] FIG. 5 shows half period graphs of switch control signals, a voltage, and a current used in the sustain-discharge driving device of FIG. 4, when a switch S_{d3} and a switch S_{d4} of the side 2 electrode of the PDP (see FIG. 7) are turned on, In this scenario, either the side 1 electrode or the side 2 electrode has a ground level potential (GND). In FIG. 5, the hatched sections do not relate to an on or off state of a gate signal. For analysis of the scenario

previously described, it is assumed that all both-end voltages at each capacitor in the energy accumulation block are sustained at the voltage $+V_s/4$ and the inductors of the energy recovery unit have the same inductance. FIGS. 6A through 6H show equivalent circuits in each mode of the sustain-discharge driving device of FIG. 4, according to the switching sequence. Hereinafter, the operations of the sustain-discharge driving device of FIG. 4 in each mode will be described with reference to FIGS. 5 through 6H.

1) Mode 1 (period t_0 through t_1; a precharging mode)

[35] Just before the time t_0, the switch S_{d1} and the switch S_{d2} are turned on, and a panel voltage V_p is sustained at 0V. The drain-source voltages of the switch S_{u1} and the switch S_{u2} are a voltage $+V_s/2$. At the time t_0, when the switch S_{d1} is turned off and the switch S_{r1} of the energy recovery unit is turned on, the capacitor C_p (PDP) is charged by the current flowing through the resonance path of the capacitor C_{d1} - the switch S_{r1} - the inductor L_{r1} - the diode D_{r1} - the switch S_{d2} - the capacitor C_p. At this time, the both-end panel voltage V_p increases from 0V to $\{(+V_s/2) - dV\}$. The voltage dV denotes a voltage drop due to a parasitic resistance of the sustain-discharge driving device. At the time t_1, when the switch S_{d2} is turned off and the switch S_{u2} is turned on, mode 1 is complete.

2) Mode 2 (period t_1 through t_2; a voltage $+V_s/2$ mode)

[36] As shown in FIG. 5, at the time t_1, the switch S_{d2} is turned off and the switch S_{u2} is turned on. The panel voltage V_p is sustained at the voltage +

$V_s/2$. The diode D_{d4} is turned on as a result of the parasitic current (free-wheeling current) generated due to reverse recovery of the diode D_{r1}, which is caused by the voltage drop of dV. As shown in FIG. 6B, the parasitic current is confined to the path of the diode D_{d4} - the inductor L_{r1}- the switch S_{r1} - the capacitor C_{d1} to suppress surge voltages of the switches. The both-end voltage at the inductor L_{r1} becomes the voltage $+V_s/4$, and thus, the parasitic current decreases rapidly at a ratio of $-V_s$ to $4L_{r1}$. In contrast, according to the conventional PDP sustain-discharge driver, the both-end voltage at the inductor is about 2V, and thus, the parasitic current decreases slowly at a ratio of –2V to 1L.

3) Mode 3 (period t_2 through t_3; a post-charging mode)

[37] At the time t_2, mode 3 starts once the switch S_{r2} is turned on. Then, as shown in FIG. 6C, the panel voltage V_p increases from the voltage $+V_s/2$ to $(+V_s\text{-}dV)$, due to a current flowing through the resonance path of the capacitor C_{d1} – the capacitor C_{d2} – the capacitor C_{u2} - the switch S_{r2} - the inductor L_{r2} - the diode D_{r2} - the switch S_{u2} - the capacitor C_p. At the time t_3, mode 3 is complete once the switch S_{u1} is turned on.

4) Mode 4 (period t_3 through t_4; a light emission mode)

[38] At the time t_3, the switch S_{u1} is turned on. As shown in FIG. 5, in mode 4, the panel voltage V_p is sustained at the voltage V_s, and a sustain-discharge current of the PDP flows through the switch S_{u1}. The duration of mode 4 is determined in relation to discharging substances of the PDP. In

general, mode 4 lasts for more than 1.7us. The diode D_{u4} is turned on by the parasitic current (free-wheeling current) generated due to reverse recovery of the diode D_{r2}, which is caused by the voltage drop of dV. As shown in FIG. 6D, the parasitic current is confined to the path of the diode D_{u4} – the inductor L_{r2} – the switch S_{r2} – the capacitor C_{u2} to suppress surge voltages of the switches. The both-end voltage at the inductor L_{r2} becomes the voltage $+V_s/4$, and thus, the parasitic current decreases rapidly at a ratio of $-V_s$ to $4L_{r2}$. In contrast, according to the conventional PDP sustain-discharge driver, the inductor both-end voltage is about 2V, and thus, the parasitic current decreases slowly at a ratio of –2V to 1L.

5) Mode 5 (period t_4 through t_5; a pre-discharging mode)

[39] At the time t_4, the switch S_{u1} is turned off and the switch S_{f2} is turned on. Thus, as shown in FIG. 6E, the panel is discharged through the resonance path of the capacitor C_p – the switch S_{u2} – the diode D_{f2} – the inductor L_{f2} – the switch S_{f2} – the capacitor C_{u2} – the capacitor C_{d2} – the capacitor C_{d1}. The panel voltage V_p decreases from the voltage $+V_s$ to the voltage $\{(+V_s/2)+dV\}$. At the time t_5, the switch S_{u2} is turned off, and mode 5 is complete.

6) Mode 6 (period t_5 through t_6; a voltage $+V_s/2$ mode)

[40] As shown in FIG. 5, at the time t_5, the switch S_{u2} is turned off and the panel voltage V_p is sustained at the voltage $+V_s/2$. The diode D_{u2} is turned on by the parasitic current (free-wheeling current) generated due to reverse recovery of the diode D_{f2}, which is caused by the voltage drop of dV. As

shown in FIG. 6F, the parasitic current is confined to the path of the switch S_{f2} – the inductor L_{f2} – the diode D_{u2} – the capacitor C_{u1} to suppress surge voltages of the switches. The both-end voltage at the inductor L_{f2} becomes the voltage $+V_s/4$, and thus, the parasitic current decreases rapidly at a ratio of $-V_s$ to $4L_{f2}$. In contrast, according to the conventional PDP sustain-discharge driver, the inductor both-end voltage is about 2V, and thus, the parasitic current decreases slowly at a ratio of –2V to 1L.

7) Mode 7 (period t_6 through t_7; a post-discharging mode)

[41] At the time t_6, once the switch S_{f1} is turned on, mode 7 starts. As shown in FIG. 6G, the panel voltage V_p decreases from the voltage $+V_s/2$ to the voltage +dV through the resonance path of the capacitor C_p – the switch S_{d2} – the diode D_{f1} – the inductor L_{f1} – the switch S_{f1} – the capacitor C_{d1}. At the time t_7, once the switch S_{d1} is turned on, mode 7 is complete.

8) Mode 8 (period t_7 through t_8; a ground mode)

[42] As shown in FIG. 5, at the time t_7, the switch S_{d1} is turned on and the panel voltage V_p becomes 0V. The diode D_{d2} is turned on by the parasitic current (free-wheeling current) generated due to reverse recovery of the diode D_{f1}, which is caused by the voltage drop of dV. As shown in FIG. 6H, the parasitic current is confined to the path of the switch S_{f1} – the inductor L_{f1} – the diode D_{d2} – the capacitor C_{d2} to suppress surge voltages of the switches. The both-end voltage at the inductor L_{f1} becomes the voltage $V_s/4$, and thus, the parasitic current decreases rapidly at a ratio of $-V_s$ to $4L_{f1}$. In contrast,

according to the conventional PDP sustain-discharge driver, the inductor both-end voltage is about 2V, and thus, the parasitic current decreases slowly at a ratio of –2V to 1L.

[43] In the manner described above, the side 2 sustain-discharge driver repeats modes 1 through 8 and applies a high-frequency AC voltage to the PDP.

[44] FIG. 7 shows a PDP driving system using the sustain-discharge driving device of the high-efficiency PDP, shown in FIG. 4. The PDP driving system includes a Y electrode sustain-discharge driving circuit 41, a separation and reset circuit 42, a scan pulse generating circuit 43, an X electrode sustain-discharge driving circuit 44, and a plasma display panel (PDP) 45.

[45] The Y electrode sustain-discharge driving circuit 41 and the X electrode sustain-discharge driving circuit 44 have already been described in FIG. 4 and will not be described here.

[46] A switch Y_p of the separation and reset circuit 42 is a switch circuit for separating circuit operations, during a sustain period, from circuit operations during other periods such as an address period and a reset period. Switches Y_{fr} and Y_{rr} of the separation and reset circuit 42 are switch circuits for applying a ramp-type high voltage to the PDP 45 during the reset period.

[47] The scan pulse generating circuit 43 applies a horizontal synchronization signal to the PDP 45 during the address period, which is shortened during other periods.

[48] Similar to the modes of the device in the FIG. 4, the charging and discharging modes during the sustain period are respectively divided into two modes, i.e., a pre-charging and post-charging mode in the charging-mode, and a pre-discharging and post-discharging mode in the discharging mode. The pre-charging and post-charging mode constitute a pair, while the pre-discharging and post-discharging mode constitute a pair. In each pair, a resonance path is formed through one of the inductors L_{r1}, L_{f1}, L_{r2}, and L_{f2}, such that the voltage stress applied to a semiconductor device is reduced. Also, by quickly eliminating the free-wheeling current, the voltage stress applied to the semiconductor device is reduced.

[49] As described above, according to the present invention, the sustain-discharge driving device of the PDP is designed to create a closed circuit in which the voltage difference between both ends of the inductor is greater than a predetermined value, thereby quickly eliminating the free-wheeling current, which is generated in the inductor of the resonance path due to a parasitic effect, during mode transition. Therefore, it is possible to reduce the current stress applied to the switches. Also, the power consumption due to the free-wheeling current can be reduced, and the timing sequence of the gate signal can be easily controlled.

[50] A method, a device, a system, etc. can implement the present invention. When the present invention is implemented through software, code segments executing essential operations constitute the present invention.

Programs or code segments are stored in a processor readable medium or transmitted by a computer data signal combined with carrier waves through a transmission medium or a communication network. The processor readable medium includes media capable of storing or transmitting information, such as electronic circuits, semiconductor memory devices, ROMs, flash memory, E^2PROMs, floppy disks, optical disks, hard disks, optical fabric media, and radio frequency (RF) networks. The computer data signal includes signals that can be transmitted through media such as electronic network channels, optical fabrics, air, electric fields, and RF networks.

[51] While the present invention has been particularly shown and described with reference to exemplary embodiments thereof, it will be understood by those of ordinary skill in the art that various changes in form and details may be made therein without departing from the spirit and scope of the present invention as defined by the following claims and their equivalents.